

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A receiver circuit for a communications terminal, comprising:

a signal-receiving device providing K analog reception signals, K being greater than one; and

a signal pre-processing circuit configured downstream from said signal-receiving device;

said pre-processing circuit including:

an analog/digital converter device having K analog/digital converters connected in parallel for sampling the K reception signals independently of one another with a sufficient sampling rate and for providing K digital signals;

a multiplexer for multiplexing the K digital signals and outputting at least one multiplexer output signal formed from the K multiplexed signals; and

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a digital filter device for filtering the at least one multiplexer output signal, said digital filter device having memory elements formed by shift registers of length K, and said digital filter device including:

a plurality of single digital filters; and

sampling rate reduction circuits configured in series in an alternating fashion.

Claims 2 - 5 (canceled).

Claim 6 (previously presented). The receiver circuit according to claim 1, wherein said digital filter device has an order of magnitude L between 5 and 20.

Claim 7 (previously presented). The receiver circuit according to claim 1, wherein said digital filter device has an order of magnitude L between 10 and 18.

Claim 8 (canceled).

Claim 9 (original). The receiver circuit according to claim 1, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal.

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Claim 10 (original). The receiver circuit according to claim 1, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal into an in-phase reception signal and a quadrature reception signal.

Claims 11-12 (canceled).

Claim 13 (previously presented). The receiver circuit according to claim 1, wherein said signal-receiving device includes a plurality of reception sensors, each of said plurality of said reception sensors has a directional reception characteristic for sensing radio signals in a predefined spatial segment.

Claim 14 (canceled).

Claim 15 (currently amended). A mobile station of a mobile radio system, comprising:

a signal-receiving device providing K analog reception signals, K being greater than one; and

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a signal pre-processing circuit configured downstream from said signal-receiving device;

said pre-processing circuit including:

an analog/digital converter device having K analog/digital converters connected in parallel for sampling the K reception signals independently of one another with a sufficient sampling rate and for providing K digital signals;

a multiplexer for multiplexing the K digital signals and outputting at least one multiplexer output signal formed from the K multiplexed signals; and

a digital filter device for filtering the at least one multiplexer output signal, said digital filter device having memory elements formed by shift registers of length K, and said digital filter device including:

a plurality of single digital filters; and

sampling rate reduction circuits configured in series in an alternating fashion.

Claims 16-18 (canceled).

Claim 19 (currently amended). A receiver circuit for a communications terminal,

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comprising:

a signal-receiving device providing K analog reception signals, K being greater than one; and

a signal pre-processing circuit configured downstream from said signal-receiving device;

said pre-processing circuit including:

an analog/digital converter device having K analog/digital converters connected in parallel for sampling the K reception signals independently of one another with a sufficient sampling rate and for providing K digital signals;

a stage containing K digital zero-inserting elements that are connected in parallel, each of said zero-inserting elements being fed with a respective one of the K digital signals and inserts K-1 zeros per sampling value of the respective one of the K digital signals into the respective one of the K digital signals; and

a digital filter device for filtering the K digital signals signal with inserted zeros, said digital filter device having memory elements formed by shift registers of length K, and said digital filter device including:

a plurality of single digital filters; and

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sampling rate reduction circuits configured in series in an alternating fashion.

Claim 20 (previously presented). The receiver circuit according to claim 19, wherein said digital filter device has an order of magnitude L between 5 and 20.

Claim 21 (previously presented). The receiver circuit according to claim 19, wherein said digital filter device has an order of magnitude L between 10 and 18.

Claim 22 (canceled).

Claim 23 (previously presented). The receiver circuit according to claim 19, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal.

Claim 24 (previously presented). The receiver circuit according to claim 19, wherein:

said signal-receiving device includes a single reception sensor outputting a single sensor reception signal; and

the K reception signals are generated by splitting the reception signal into an in-

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phase reception signal and a quadrature reception signal.

Claim 25 (previously presented). The receiver circuit according to claim 19, wherein said signal-receiving device includes a plurality of reception sensors, each of said plurality of said reception sensors has a directional reception characteristic for sensing radio signals in a predefined spatial segment.

Claim 26 (canceled).

Claim 27 (new). A receiver circuit for a communications terminal, comprising:

a signal-receiving device providing K analog reception signals, K being greater than one; and

a signal pre-processing circuit configured downstream from said signal-receiving device, said signal pre-processing circuit including:

an analog/digital converter device having K analog/digital converters connected in parallel for sampling the K reception signals independently of one another with a sufficient sampling rate and for providing K digital signals;

a stage containing K digital zero-inserting elements that are connected in parallel, each of said zero-inserting elements being fed with a respective one of the K digital signals and inserting K - 1 zeros per sampling value of the

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respective one of the K digital signals into the respective one of the K digital signals; and

a digital filter device for filtering the K digital signals with inserted zeros, said digital filter device having K inputs, wherein a k-th input, $k = 1, \dots, K$, respectively, is connected to a series of

a number of $k - 1$ leading memory locations; and

a given number of following memory elements each formed by shift registers of a length of K memory locations.